NNIPREIOTRISCV50

20µW 50Mbps IoT RISCV Co-Processor

Product Brief

Features

- Implements RISCV core
- 20µW maximum power consumption
- Maximum throughput of 50Mbps
- Handles all wireless sensor node processing in one IP core
- Supports high-performance and low power operating modes.
- Optimized for Xilinx FPGA kits
- Optimized for multiplexing and sensor fusion applications

Applications

- Low power tiny area IoT RISC-V co-processor for biomedical, body area network, wearable, and sensor fusion applications.

Description

The NNIPREIOTRISCV50 soft IP is intended to be used in Xilinx FPGA kits as an RTL optimized code. In addition, it is available as a hard ASIC IP which can be cost-effectively ported across process nodes and technology foundries.

The hard ASIC IP provides up to 50Mbps throughput with power consumption of 20µW and very small Silicon area.

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IP Deliverables

- Datasheet
- RTL code for the soft IP core
- Layout View (gds2) for the hard ASIC IP core
- Integration Support

Najah Now IP

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NajahNow Digital hard IP cores have been silicon verified in a number of foundries (TSMC, Global Foundries, UMC, and Fujitsu) at nodes ranging from 180nm to 18nm.